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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,575	06/24/2003	Martin Robert Evans	550-445	8224

23117 7590 06/18/2007

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EXAMINER	
LAI, VINCENT	
ART UNIT	**PAPER NUMBER**
2181	
MAIL DATE	**DELIVERY MODE**
06/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/601,575	EVANS ET AL.	
	Examiner	Art Unit	
	Vincent Lai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/18/06*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *Herewith*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Acknowledgment is made of the amendment of the specification filed by applicant on 6 April 2006

Information Disclosure Statement

2. The information disclosure statements (IDS) submitted on 8 January 2004 and 18 December 2006 was considered by the examiner.

Response to Arguments

3. In view of the Appeal Brief filed on 17 January 2007, PROSECUTION IS HEREBY REOPENED. A new ground rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

Response to Arguments

3. The Examiner notes an error was made in the Final Office Action mailed 31 May 2006 and the objection to the title was repeated. Objection to the title has been withdrawn after considering amendment.

4. Applicant's arguments with respect to claims 1-45 have been considered but are moot in view of the new ground(s) of rejection.

It is noted that the new grounds of rejection is similar to Japanese Publication # JP-2001-147809, a reference found in the IDS submitted 18 December 2006, and shares a common inventory (Margaret Rose Gearty).

Drawings

5. The drawings remain objected to, although previously indicated errors have been corrected, because the newly submitted drawings do not include any labels indicated that the drawings have been amended (See 37 CFR 1.84).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-45 are rejected under 35 U.S.C. 102(e) as being anticipated by Gearty et al (U.S. Patent # 6,477,638 B1), herein referred to as Gearty.

As per **claim 1**, Gearty discloses a data processing apparatus, comprising:

a main processor operable to execute a sequence of instructions (See column 6, lines 29-30: A sequence of instructions is sent to the CPU), the main processor comprising a first pipeline having a first plurality of pipeline stages (See figure 3 and column 6, lines 14-28: A pipeline with many stages is taught);

a coprocessor operable to execute coprocessor instructions in said sequence of instructions (See figure 2 and column 5, lines 44-48: the FPU is the coprocessor), the coprocessor comprising a second pipeline having a second plurality of pipeline stages (See figure 3 and column 6, lines 14-28: A pipeline with many stages is taught), and each coprocessor instruction being arranged to be routed through both the first pipeline

and the second pipeline (See column 6, lines 29-30: A sequence of instructions is sent to both the CPU and the FPU); and

at least one synchronising queue coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines (See figure 6, and column 11, lines 19-30: A connection between decoder stages exists), the predetermined pipeline stage being operable to cause a token to be placed in the synchronising queue when processing a coprocessor instruction and the partner pipeline stage being operable to process that coprocessor instruction upon receipt of the token from the synchronising queue, thereby synchronising the first and second pipelines between the predetermined pipeline stage and the partner pipeline stage (See column 11, lines 1-18: A "go-token" is taught which is use to synchronize the pipelines).

As per **claim 2**, Gearty discloses a plurality of said synchronising queues, each said synchronising queue coupling a predetermined pipeline stage in one of the pipelines with a partner pipeline stage in the other of the pipelines (See figure 4 and column 9, lines 31-48: The stages are connected for synchronization purposes).

As per **claim 3**, Gearty discloses wherein one of the at least one synchronising queues is an instruction queue (See column 11, lines 62-67: Instruction queues have to be synchronized), the predetermined pipeline stage is in the first pipeline and is arranged to cause a token identifying a coprocessor instruction to be placed in the instruction queue (See column 11, lines 1-18: A "go-token" is taught which is use to

synchronize the pipelines), and the partner pipeline stage is in the second pipeline and is operable upon receipt of the token to begin processing the coprocessor instruction identified by the token (See column 13, lines 14-35: The coprocessor starts when the go-token instructs it to).

As per **claim 4**, Gearty discloses wherein the predetermined pipeline stage is a fetch stage in the first pipeline and the partner pipeline stage is a decode stage in the second pipeline, that decode stage being operable to decode the coprocessor instruction upon receipt of the token (See figure 4: The fetch stage of the first pipeline and the decode stage of the second are connected and the second pipeline can decode instructions that are sent by the first pipeline).

As per **claim 5**, Gearty discloses wherein the fetch stage in the first pipeline is operable to cause a token to be placed in the instruction queue for each instruction in the sequence of instructions (See column 11, lines 1-18: A "go-token" is taught which is use to synchronize the pipelines), and the decode stage in the second pipeline is arranged to decode each instruction upon receipt of the associated token in order to determine whether that instruction is a coprocessor instruction that requires further processing by the coprocessor (See figure 4: The fetch stage of the first pipeline and the decode stage of the second are connected and the second pipeline can decode instructions that are sent by the first pipeline).

As per **claim 6**, Gearty discloses wherein one of the at least one synchronising queues is a cancel queue (See column 7 & 8: The table shows the ifu_fpu_cancel_wb queue which is used to cancel instructions), the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the cancel queue a token identifying whether a coprocessor instruction at that predetermined pipeline stage is to be cancelled (See column 7 & 8: The table shows the ifu_fpu_cancel_wb queue associates itself with an instruction), and the partner pipeline stage is in the second pipeline and is operable upon receipt of the token from the cancel queue , and if the token identifies that the coprocessor instruction is to be cancelled, to cause that coprocessor instruction to be cancelled (See column 7 & 8: A cancellation will be done on the associated instruction with the ifu_fpu_cancel_wb queue).

As per **claim 7**, Gearty discloses wherein the predetermined pipeline stage is an issue stage in the first pipeline, and the partner pipeline stage is a stage following an issue stage in the second pipeline (See figure 3: The issue stage is associated with the fetch stage and from the figure, a natural association/connection is present with the fetch stages of both pipelines).

As per **claim 8**, Gearty discloses wherein the partner pipeline stage is operable upon receipt of the token from the cancel queue (See column 7 & 8: The table shows the ifu_fpu_cancel_wb queue which is used to cancel instructions), and if the token identifies that the coprocessor instruction is to be cancelled, to remove the coprocessor

instruction from the second pipeline (See column 7 & 8: A cancellation will be done on the associated instruction with the ifu_fpu_cancel_wb queue).

As per **claim 9**, Gearty discloses wherein one of the at least one synchronising queues is a finish queue (See column 7 & 8: The table shows the ifu_fpu_data_wb queue which is used to complete instructions), the predetermined pipeline stage is in the first pipeline and is arranged to cause to be placed in the finish queue a token identifying permission for a coprocessor instruction at that predetermined pipeline stage to be retired from the second pipeline (See column 7 & 8: The ifu_fpu_data_wb queue associates itself with the instructions to be completed), and the partner pipeline stage is in the second pipeline and is operable upon receipt of the token from the finish queue, and if the token identifies that the coprocessor instruction is permitted to be retired, to cause that coprocessor instruction to be retired (See column 7 & 8: The instructions in the ifu_fpu_data_wb queue will be completed).

As per **claim 10**, Gearty discloses wherein the predetermined pipeline stage is a write back stage in the first pipeline, and the partner pipeline stage is a write back stage in the second pipeline (See column 7 & 8: The ifu_fpu_data_wb queue associates the two write back stages).

As per **claim 11**, Gearty discloses wherein one of the at least one synchronising queues is a length queue, the predetermined pipeline stage is in the second pipeline

and is arranged, for a vectored coprocessor instruction, to cause to be placed in the length queue a token identifying length information for the vectored coprocessor instruction, and the partner pipeline stage is in the first pipeline and is operable upon receipt of the token from the length queue to factor the length information into the further processing of the vectored coprocessor instruction within the first pipeline (See column 5, lines 54-59: Module 124 can be used for vector processing).

As per **claim 12**, Gearty discloses wherein the predetermined pipeline stage is a decode stage in the second pipeline, and the partner pipeline stage is a first execute stage in the first pipeline (See figure 4: A connection exists between the decode stage in the second pipeline, and the execute stage in the first pipeline).

As per **claim 13**, Gearty discloses wherein one of the at least one synchronising queues is an accept queue, the predetermined pipeline stage is in the second pipeline and is arranged to cause to be placed in the accept queue a token identifying whether a coprocessor instruction in that predetermined pipeline stage is to be accepted for execution by the coprocessor, and the partner pipeline stage is in the first pipeline and is operable upon receipt of the token from the accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to cause that coprocessor instruction to be rejected by the main processor (See column 10, lines 14-20: An accept signal is taught and no further instructions are issued until an accept signal is received).

As per **claim 14**, Gearty discloses wherein the predetermined pipeline stage is an issue stage in the second pipeline, and the partner pipeline stage is a second execute stage in the first pipeline (See column 10, lines 14-20: An accept signal is taught and no further instructions are issued until an accept signal is received).

As per **claim 15**, Gearty discloses wherein the partner pipeline stage is operable upon receipt of the token from the accept queue, and if the token identifies that the coprocessor instruction is not to be accepted, to remove the coprocessor instruction from the first pipeline (See column 10, lines 14-20: An accept signal is taught and no further instructions are issued until an accept signal is received)

As per **claim 16**, Gearty discloses wherein one of the at least one synchronising queues is a store queue used when the coprocessor instruction is a store instruction operable to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is operable upon receipt of each token from the store queue, to cause the corresponding data item to be transferred to the memory (See column 12, lines 37-67: A store is done utilizing a token and synchronization of the two pipelines).

As per **claim 17**, Gearty discloses wherein the predetermined pipeline stage is an issue stage in the second pipeline, and the partner pipeline stage is an address generation stage in the first pipeline (See figure 3: The issue stage and address generation is associated with the fetch stage and from the figure, a natural association/connection is present with the fetch stages of both pipelines).

As per **claim 18**, Gearty discloses wherein one of the at least one synchronising queues is a load queue used when the coprocessor instruction is a load instruction operable to cause data items to be transferred from memory accessible by the main processor to the coprocessor, the predetermined pipeline stage is in the first pipeline and is arranged, when processing one of said load instructions, to cause to be placed in the load queue a token identifying each data item to be transferred, and the partner pipeline stage is in the second pipeline and is operable upon receipt of each token from the load queue, to cause the corresponding data item to be transferred to the coprocessor (See column 12, lines 37-67: A load is done utilizing a token and synchronization of the two pipelines).

As per **claim 19**, Gearty discloses wherein the predetermined pipeline stage is a write back stage in the first pipeline, and the partner pipeline stage is a write back stage in the second pipeline (See column 7 & 8: The ifu_fpu_data_wb queue associates the two write back stages).

As per **claim 20**, Gearty discloses wherein one of the at least one synchronising queues is a store queue used when the coprocessor instruction is a store instruction operable to cause data items to be transferred from the coprocessor to memory accessible by the main processor, the predetermined pipeline stage is in the second pipeline and is arranged, when processing one of said store instructions, to cause to be placed in the store queue a token identifying each data item to be transferred, and the partner pipeline stage is in the first pipeline and is operable upon receipt of each token from the store queue, to cause the corresponding data item to be transferred to the memory, and wherein the load instruction and store instruction may be vectored coprocessor instructions defining multiple data items to be transferred, and the apparatus further comprises flow control logic, associated with at least one of the load queue and the store queue, operable to send a control signal to the predetermined pipeline stage to stop issuance of tokens by the predetermined pipeline stage whilst it is determined that the associated load or store queue may become full (See column 12, lines 37-67: A store is done utilizing a token and synchronization of the two pipelines).

As per **claim 21**, Gearty discloses wherein the flow control logic is provided for the store queue, the flow control logic being operable to issue the control signal upon receiving an indication from the main processor that the partner pipeline stage cannot accept a data item (See column 12, lines 37-67: A token is used to indicate status).

As per **claim 22**, Gearty discloses wherein the load queue is a double buffer (See figure 5 and column 10, lines 11-13: The load queue recirculates).

As per **claim 23**, Gearty discloses wherein each token includes a tag which identifies the coprocessor instruction to which the token relates (See column 7 & 8: All tokens have associates itself with an instruction).

As per **claim 24**, Gearty discloses wherein the main processor is operable, when it is necessary to flush coprocessor instructions from both the first and the second pipeline, to broadcast a flush signal to the coprocessor identifying the tag relating to the oldest instruction that needs to be flushed, the coprocessor being operable to identify that oldest instruction from the tag and to flush from the second pipeline that oldest instruction and any later instructions within the coprocessor (See column 7, lines 6-48: The state can be cleared or flushed).

As per **claim 25**, Gearty discloses wherein one or more of said at least one synchronising queues are flushed in response to said flush signal, with the tag being used to identify which tokens within the queue are to be flushed (See column 7, lines 6-48: The state can be cleared or flushed).

As per **claim 26**, Gearty discloses wherein the at least one synchronising queue comprises a First-In-First-Out (FIFO) buffer having a predetermined number of entries

for storing tokens (See figure 5 and column 10, lines 11-13: Although a FIFO is not explicitly taught, the teaching of recirculation indicates that a FIFO is used for the buffer).

As per **claim 27**, Gearty discloses wherein a plurality of said coprocessors are provided, with each synchronising queue coupling a pipeline stage in the main processor with a pipeline stage in one of the coprocessors (See column 1, lines 14-26: Gearty teaches chips may have multiple modules, modules which can be FPUs).

As per **claim 28** Gearty discloses wherein the data processing apparatus has a synchronous design, such that the tokens are caused to be placed in the queue by the predetermined pipeline stage and are caused to be received from the queue by the partner pipeline stage upon changing edges of a clock cycle (See column 9, lines 39-47: The system is run generally in a synchronous fashion and is out of sync in only rare circumstances).

Claim 29 is rejected for reasons similar to that of claim 1. Claim 29 is the method claim for the apparatus of claim 1.

Claim 30 is rejected for reasons similar to that of claims 2, 4, 7, 10, 12, 14, 17, and 19. Claim 30 is the method claim for the apparatus of claims 2, 4, 7, 10, 12, 14, 17, and 19.

Claims 31-45 is rejected for reasons similar to that of claim 3, 6, 9, 11, 13, 16, 18, 20, 21, and 23-28, respectively. Claims 31-45 are the method claim for the apparatus of claim 3, 6, 9, 11, 13, 16, 18, 20, 21, and 23-28, respectively.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent Lai whose telephone number is (571) 272-6749. The examiner can normally be reached on M-F 8:00-5:30 (First BiWeek Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vincent Lai
Examiner
Art Unit 2181

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May 23, 2007